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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/681,126	10/09/2003	Hidekatsu Onose	500.43193X00	8090

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/681,126	ONOSE ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

KD

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, 6, and 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,747,831 to Loose et al.

Regarding claims 1 and 10, Loose discloses a substrate/drift region of a first (n) conduction type with a low impurity concentration (see figure 3; also, column 2, lines 50-51) and a bandgap of 2.0 eV or higher (layers of SiC have a bandgap higher than 2.0 eV; column 2, lines 40-52); a first region/drain region (drain in figure 3) formed in a first plane of the substrate and having the same conduction type (n; figures 2h and 3) and a lower resistance (figure 3) than the substrate; a first electrode/drain electrode (column 2, lines 51-53) formed in another plane of the first region; a second region/source region (1) formed in a second plane of the substrate (figure 2A) and having the same conduction type (n; figure 3) as the substrate; and a second electrode/source electrode (6) formed in the second region (figures 2h; 3), the device comprising: a trench formed in the second plane of the substrate (figure 2b); a control region/gate region (2,3) formed from a bottom of the trench into the substrate (figures 2h, 3) and having a different

conduction type (p) than that of the substrate (figure 3); a control electrode/gate electrode (4) formed in the control region (figures 2h, 3); and the second electrode formed over the control electrode through an insulating film (5; figures 2f-2h).

Regarding claim 2, Loose discloses that the control region is formed in at least a part of the sidewall of the trench (figures 2h, 3).

Regarding claim 6, Loose discloses that the width of the control region is narrower on the second region side (top side) than on the first region side (bottom side; see figure 3).

Regarding claim 8, Loose discloses that the control region in contact with the sidewall of the trench is formed with a Schottky contact to provide a MESFET (column 3, lines 20-25).

Regarding claim 9, Loose discloses that the second electrode (6) is formed over an entire surface of the unit device (figure 2h).

3. Claim 10 is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,617,653 to Yokogawa et al.

Yokogawa discloses an n-type drift region (41) with a low impurity concentration (figure 11c) having a band gap of 2.0 eV or higher (column 15, lines 1-10); an n-type drain region (40) in a first plane of the drift region and having a lower resistance than the drift region (figure 11c); a drain electrode (50) formed in another plane of the first region; an n-type source region (44) formed in a second plane of the drift region (figure 11c); and a drain electrode (49) in the second region, the device comprising: a trench formed in the second plane of the drift region (figure 10b); a p-type gate region (43; column 15, lines 30-42) formed from a bottom of the trench into the drift region (figure 11c); a gate electrode (47) formed in the gate region (figures 11a-11c);

and the source electrode formed over the gate electrode through an insulating film (48; figures 11b-11c).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5, 7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yokogawa et al. in view of U.S. Patent No. 6,380,569 to Chang et al.

Regarding claim 1, Yokogawa discloses a drift region (41) of a first impurity type (n) having a band gap of 2.0 eV or higher (column 15, lines 1-10) and a low impurity concentration (figure 11c); a first region (drain region 40) in a first plane of the drift region and having the same conduction type (n) as the drift region and a lower resistance (figure 11c); a first electrode (50) formed in another plane of the first region; a second region (44) formed in a second plane of the drift region (figure 11c) and having the same conduction type (n) as the drift region; and a second electrode (49) in the second region, the device comprising: a trench formed in the second plane of the drift region (figure 10b); a control region (43) formed from a bottom of the trench into the drift region (figure 11c) and having a different conduction type than the drift region (column 15, lines 30-42); a control electrode (47) formed in the control region (figures 11a-11c);

and the second electrode formed over the control electrode through an insulating film (48; figures 11b-11c).

Yokogawa fails to disclose that the drift region, rather than the drain region, is the substrate material.

Chang discloses that substantially the same FET structures can be formed by using an NPT wafer (the drift layer is the substrate, and the drain region at the bottom is provided by implanting dopants; see column 7, lines 25-44) or by using an epitaxial wafer (highly doped drain layer is the substrate, and the drift region is epitaxially grown; see column 4, lines 5-28; also see figure 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the structure of Yokogawa, such that an NPT wafer is used, rather than an epitaxial wafer, as suggested by Chang. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use an NPT wafer rather than an epitaxial wafer, because Chang shows that substantially the same device structure results with either type of wafer, but that the NPT wafer is cheaper than an epitaxial wafer (see Chang, column 7, lines 25-44). Since both Yokogawa and Chang teach similar structures (see figures 6a, 6b of Chang, and 11c of Yokogawa), a person having ordinary skill in the art would expect that the substitution of an NPT wafer for the epitaxial wafer of Yokogawa would produce substantially identical structures, and hence would select the NPT wafer to decrease the production cost.

Regarding claim 2, Yokogawa discloses that the control region is formed in at least part of the sidewall (figure 11c).

Regarding claim 3, Yokogawa discloses that the control region (43) is in contact with the second region (44; figure 11c).

Regarding claim 4, Yokogawa discloses that the channel between the control regions only extends across the bottom half of the trench (see figure 11c), and hence, the narrowest portion (and the entire channel region) must be deeper than half of the depth of the control region.

Regarding claims 5 and 7, Yokogawa discloses that an insulating film (46) is formed between the sidewall and the control region (figure 11c), thus forming a MOS channel (figure 11c).

Regarding claim 9, Yokogawa discloses that the second electrode is formed over an entire surface of the unit device (figure 11c).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,396,085 to Baliga discloses a SiC device with a control region extending around the bottom of a trench.

b. U.S. Patent No. 5,945,701 to Siergiej et al. and U.S. Patent No. 5,753,938 to Thapar et al. disclose static induction transistors having p-type material disposed in the lower regions of a trench.

c. U.S. Patent No. 6,767,783 to Casady et al. discloses SiC transistor structures having implanted gate regions at the bottom of a trench.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

CARL WHITEHEAD JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800